Lab #18 Name: _____ Per: _____

Title: THE UNIVERSAL SHIFT REGISTER

Materials:
[2] 74194 4-bit bi-directional universal shift register ICs
[1] clock (single pulse)

Procedure:

1. Using the diagram done in class (or page 193 of your textbook and a pinout diagram for a 74194), fill in Chart 1. Wire the 74194 as a 4-bit, **serial load, shift-right** register using the pin data from Chart 1.
2. Operate the switches according to Table 18-3 and fill in the "Shift right register" output column. **Get Instructor's Signature.**
3. Using the diagram done in class (or page 193 of your textbook and a pinout diagram for a 74194), fill in Chart 2. Wire the 74194 as a 4-bit, **serial load, shift-left** register using the pin data from Chart 2.
4. Operate the switches according to Table 18-3 and fill in the "Shift left register" output column. **Get Instructor's Signature.**
5. Using the diagram done in class (or page 194 of your textbook and a pinout diagram for a 74194), fill in Chart 3. Wire the 74194 as a 4-bit, **parallel load, shift-right/left** register using the pin data from Chart 3.
6. Operate the switches according to Table 18-4 and fill in the output columns. **Get Instructor's Signature.**
7. Possible Bonus (ask your instructor): On page 194 of your textbook there is a diagram of an 8-bit parallel load shift-right register. Wire it and explain to your instructor how it works.

Questions: (answer on a separate piece of paper – **"Draw" means you must use a template**):

1. The CLR input on the 74914 IC is enabled by a logical _____ (0, 1).
2. The data inputs (shift right, shift left, parallel) on the 74194 IC are all _____ (asynchronous, synchronous) inputs.
3. List the four modes of operation for the 74194 IC and the input conditions of S_0 and S_1 to produce these modes.
4. Refer to lines 12 and 13 in the Shift Right columns of Table 18-3. Why did the register not go to 0111 in line 13 as the register shifted right?
5. Refer to Table 18-3. Explain how you would enter 0110 in a serial shift register (74194).
6. Refer to Table 18-4. Explain how you would enter 0110 in a parallel load shift register (74194).
7. Explain how you would enter 00110110 in an 8-bit parallel load shift register (2 74194 ICs).
8. Refer to Table 18-4, line 1. Why do all inputs except the CLR input show an X (irrelevant)?
9. Refer to Table 18-4, lines 27 and 28. The Mode control would be in what position in these lines?
10. Refer to Table 18-4. Why is there no shift from line 15 to 16 even if there is a clock pulse?

Chart 1

4-Bit, Serial Load, Shift-Right Register

A switch for the serial input (<u>shift right</u>) goes to	pin ___
A clock for the CLK input goes to	pin ___
A switch for the CLR input goes to	pin ___
A switch for the mode control S_0 goes to	pin ___ and
should be set to a ____(0, 1).	
A switch for the mode control S_1 goes to	pin ___ and
should be set to a ____(0, 1).	
+5V should go to	pin ___
GND should go to	pin ___
The 4 LEDs (Q_A, Q_B, Q_C, Q_D) should come from	pin ___ and
	pin ___ and
	pin ___ and
	pin ___

Chart 2

4-Bit, Serial Load, Shift-Left Register

A switch for the serial input (<u>shift left</u>) goes to	pin ___
A clock for the CLK input goes to	pin ___
A switch for the CLR input goes to	pin ___
A switch for the mode control S_0 goes to	pin ___ and
should be set to a ____(0, 1).	
A switch for the mode control S_1 goes to	pin ___ and
should be set to a ____(0, 1).	
+5V should go to	pin ___
GND should go to	pin ___
The 4 LEDs (Q_A, Q_B, Q_C, Q_D) should come from	pin ___ and
	pin ___ and
	pin ___ and
	pin ___

Chart 3

4-Bit, Parallel Load, Shift-Right/Left Register

4 switches for the parallel inputs (A,B,C,D) go to	pin ___ and
	pin ___ and
	pin ___ and
	pin ___
A switch for the serial input (shift right) goes to	pin ___
A switch for the serial input (shift left) goes to	pin ___
A clock for the CLK input goes to	pin ___
A switch for the CLR input goes to	pin ___
A switch for the mode control S_0 goes to	pin ___
A switch for the mode control S_1 goes to	pin ___
+5V should go to	pin ___
GND should go to	pin ___
The 4 LEDs (Q_A, Q_B, Q_C, Q_D) should come from	pin ___ and
	pin ___ and
	pin ___ and
	pin ___

The 3 modes that will be used for this part are:

Parallel Load,	which has S_0=___ and S_1=___
Shift Right,	which has S_0=___ and S_1=___
Shift Left,	which has S_0=___ and S_1=___

Inputs				Outputs							
Line	Clear	Data serial input	Clock pulse number	Shift Right register				Shift Left register			
				A	B	C	D	A	B	C	D
1	0	1	0	0	0	0	0	0	0	0	0
2	1	1	0								
3	1	1	1								
4	1	0	2								
5	1	0	3								
6	1	0	4								
7	1	0	5								
8	1	1									
9	1	1	6								
10	1	1	7								
11	1	1	8								
12	1	1	9								
13	1	1	10								
14	1	0	11								
15	1	0	12								
16	1	0	13								
17	1	0	14								
18	1	1									
19	1	1	15								
20	1	1	16								
21	1	0	17								
22	1	0	18								
23	1	0	19								
24	1	0	20								

Table 18-3 Serial Shift Registers

Inputs											Outputs			
Line	Mode Control		Clear	Shift left serial input	Shift right serial input	Data Parallel inputs				clock pulse number	4-bit shift register			
	S_0	S_1				A	B	C	D		A	B	C	D
1	X	X	0	X	X	X	X	X	X	0	0	0	0	0
2	1	1	1	X	X	0	1	0	0	0				
3	1	1	1	X	X	0	1	0	0	1				
4	1	0	1	X	0	X	X	X	X	2				
5	1	0	1	X	0	X	X	X	X	3				
6	1	0	1	X	0	X	X	X	X	4				
7	1	1	1	X	X	0	1	1	0					
8	1	0	1	X	0	0	1	1	0	5				
9	1	0	1	X	1	X	X	X	X	6				
10	1	0	1	X	1	X	X	X	X	7				
11	1	0	1	X	1	X	X	X	X	8				
12	1	0	1	X	1	X	X	X	X	9				
13	X	X	0	X	X	X	X	X	X					
14	1	1	1	X	X	1	0	1	0					
15	1	1	1	X	X	1	0	1	0	10				
16	1	1	1	X	0	1	0	1	0	11				
17	1	0	1	X	0	X	X	X	X	12				
18	1	0	1	X	0	X	X	X	X	13				
19	1	0	1	X	0	X	X	X	X	14				
20	1	0	1	X	0	X	X	X	X	15				
21	1	1	1	X	X	0	0	0	1	16				
22	0	1	1	0	X	X	X	X	X	17				
23	0	1	1	0	X	X	X	X	X	18				
24	0	1	1	0	X	X	X	X	X	19				
25	0	1	1	0	X	X	X	X	X	20				
26	1	1	1	X	X	0	1	1	0	21				
27	0	0	1	0	0	X	X	X	X	22				
28	0	0	1	0	0	X	X	X	X	23				
29	0	1	1	0	0	X	X	X	X	24				
30	1	0	1	0	0	X	X	X	X	25				

Table 18-4 Parallel-load shift right/left register