

Lab #3

Name: \_\_\_\_\_ Per: \_\_\_\_\_

Title: **OR GATES**

Materials:

- [1] 7432 2-input OR gate IC
- [1] led with 150-Ω resistor
- [5] logic switches

Procedure:

1. Insert the 7432 IC into the breadboard.
2. Connect power to the 7432: red wire for +5V( $V_{cc}$ ) and the black wire for GND.
3. Refer to Fig. 3-5. Wire the 2-input OR gate (see pinout diagram).
4. Move input switches A and B to each combination shown in the left side of the truth table in Table 3-4. Observe and record the results in the OR gate 1 column. Record a logical 0 if the light is OFF; record a logical 1 if the light is ON.
5. Now wire and test each of the other three OR gates packaged inside the 7432 IC. Record their outputs in the right-hand columns of Table 3-4. Record 0's and 1's. **Get Instructor's Signature. (all 4 gates should be wired with a separate pair of switches and an led for each)**
6. Wire the 5-input OR gate using all four 2-input OR gates in the 7432. Pin numbers are shown in Fig. 3-6.
7. Operate and observe the output of the 5-input OR gate as you place the input switches (A-E) in the 32 different combinations in the Input column of Table 3-5. Record the outputs in the Output column of Table 3-5. **Get Instructor's Signature.**

Questions (answer on a separate piece of paper – “Draw” means you must use a template):

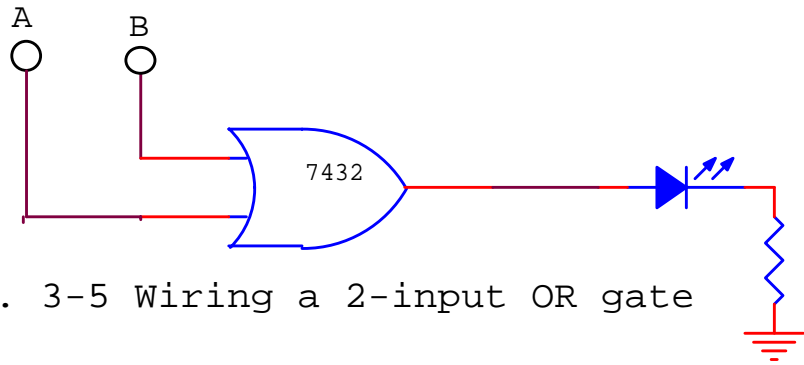
1. **Draw** a single logic symbol for the 5-input OR gate you wired in this experiment. Label the inputs A, B, C, D, and E; label the output Y.
2. **Draw** a logic diagram of a 3-input OR gate using two 2-input OR gates. Label the inputs A, B, and C; label the output Y.
3. **Draw** the truth table for a 3-input OR gate. Fill in the truth table completely.
4. When powering the IC in this experiment, the GND is connected to the \_\_\_\_\_ of the power supply.
5. A logical 0 on the truth table in this experiment means that input or output is \_\_\_\_\_ (near GND, near +5V).
6. A logical 1 on the truth table in this experiment means that input or output is \_\_\_\_\_ (near GND, near +5V).
7. A truth table with two inputs has how many switch combinations?
8. A truth table with three inputs has how many switch combinations?
9. A truth table with five inputs has how many switch combinations?
10. The OR gates unique output is a \_\_\_\_\_(0,1), which only occurs when all inputs are \_\_\_\_\_ (high, low).

| Inputs |   | Outputs   |           |           |           |
|--------|---|-----------|-----------|-----------|-----------|
| A      | B | OR gate 1 | OR gate 2 | OR gate 3 | OR gate 4 |
| 0      | 0 |           |           |           |           |
| 0      | 1 |           |           |           |           |
| 1      | 0 |           |           |           |           |
| 1      | 1 |           |           |           |           |

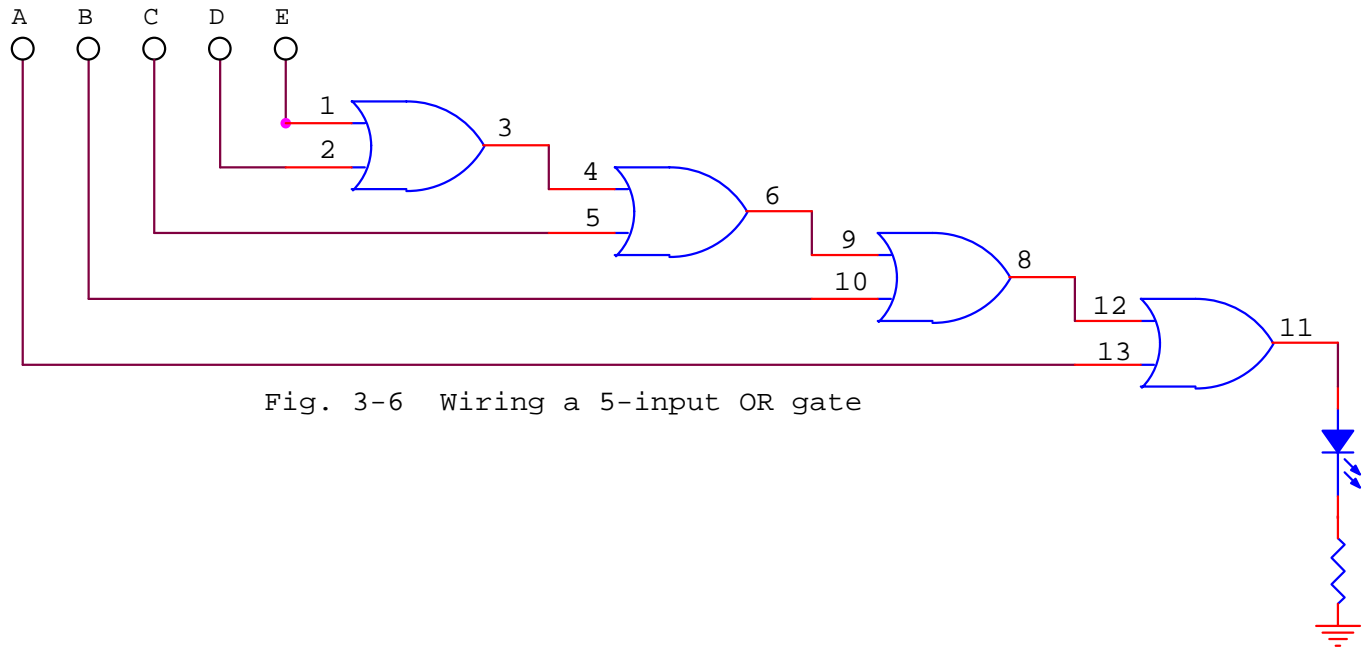
Table 3-4 Truth Table for 7432

**Table 3-5 5-input OR gate**

| INPUTS |   |   |   |   | OUTPUTS |
|--------|---|---|---|---|---------|
| A      | B | C | D | E |         |
| 0      | 0 | 0 | 0 | 0 |         |
| 0      | 0 | 0 | 0 | 1 |         |
| 0      | 0 | 0 | 1 | 0 |         |
| 0      | 0 | 0 | 1 | 1 |         |
| 0      | 0 | 1 | 0 | 0 |         |
| 0      | 0 | 1 | 0 | 1 |         |
| 0      | 0 | 1 | 1 | 0 |         |
| 0      | 0 | 1 | 1 | 1 |         |
| 0      | 1 | 0 | 0 | 0 |         |
| 0      | 1 | 0 | 0 | 1 |         |
| 0      | 1 | 0 | 1 | 0 |         |
| 0      | 1 | 0 | 1 | 1 |         |
| 0      | 1 | 1 | 0 | 0 |         |
| 0      | 1 | 1 | 0 | 1 |         |
| 0      | 1 | 1 | 1 | 0 |         |
| 0      | 1 | 1 | 1 | 1 |         |
| 1      | 0 | 0 | 0 | 0 |         |
| 1      | 0 | 0 | 0 | 1 |         |
| 1      | 0 | 0 | 1 | 0 |         |
| 1      | 0 | 0 | 1 | 1 |         |
| 1      | 0 | 1 | 0 | 0 |         |
| 1      | 0 | 1 | 0 | 1 |         |
| 1      | 0 | 1 | 1 | 0 |         |
| 1      | 0 | 1 | 1 | 1 |         |
| 1      | 1 | 0 | 0 | 0 |         |
| 1      | 1 | 0 | 0 | 1 |         |
| 1      | 1 | 0 | 1 | 0 |         |
| 1      | 1 | 0 | 1 | 1 |         |
| 1      | 1 | 1 | 0 | 0 |         |
| 1      | 1 | 1 | 0 | 1 |         |
| 1      | 1 | 1 | 1 | 0 |         |
| 1      | 1 | 1 | 1 | 1 |         |



**Fig. 3-5 Wiring a 2-input OR gate**



**Fig. 3-6 Wiring a 5-input OR gate**

